REMARKS

Favorable consideration and allowance of the claims of the present application are respectfully requested.

In the present Official Action, the Examiner had rejected Claims 1, 2, 7, 8, 13 and 17-19 and 23-25 under 35 U.S.C. §102(e) as allegedly anticipated by Nadeau-Dostie et al. (US Patent Pub. No. 2005/0047229) ("Nadeau-Dostie").

Further, Claims 3-6, 9-12, 14-16 and 20-22 were rejected under 35 U.S.C. §103(a) as allegedly unpatentable over Nadeau-Dostie in further view of US Patent No. 6,978,402 to Hirabayashi ("Hirabayashi ").

As a preliminary matter, Claims 7-12 are being canceled herein. Claims 17-20 are being canceled herein and the subject matter thereof being added to Claim 21, now re-cast in independent form to include all of the canceled claim limitations. Applicants respectfully reserve the right to follow any continuation or divisional patent application directed to those canceled claims.

With respect to the rejection of Claims 1, 2, 13 and 17-19 and 23-25 under 35 U.S.C. §102(e) as allegedly anticipated by Nadeau-Dostie, applicants respectfully traverse in view of the amendments made herein to Claims 1, 13 and 17 that distinguish the present invention over Nadeau-Dostie.

Particularly, these independent claims are being amended to highlight important features of the invention as exemplified by Claim 1 as amended with new limitations (underlined) that now sets forth:

A method for implementing at speed bit fail mapping of an embedded memory system having a BIST (Built In Self Testing) engine, comprising:

using a high speed multiplied clock which is an asynchronous multiple of [[an]] a slower external clock of a tester to sequence BIST bit fail testing of the embedded memory system, said BIST generating a fail map data including all diagnostic fails for capture by a diagnostic register device under control of said high speed multiplied clock, the diagnostic fail data being stored in fail location latches of said diagnostic register device at a time of recognizing said BIST fail test;

generating a signal for receipt by said tester to identify a BIST bit fail test for said tester, and;

in response to said generated signal, implementing a BIST clock control logic for automatically pausing the BIST bit fail testing upon recognition of a fail of the embedded memory system, said BIST clock control logic gating off said high speed multiplied clock to BIST test latches and fail location latches of said diagnostic register;

receiving, from said tester, a first signal asserted in response to receiving said generated signal;

said BIST clock control logic automatically switching, in response to said received asserted first signal, said diagnostic register device to operate from a data capture mode controlled by the high speed multiplied clock to a serial transfer mode controlled by the slower external clock of the tester;

using the slower external clock of the tester to read bit fail data out from said fail location latches of said diagnostic register device to the tester; and,

receiving, from said tester, a de-asserted first signal when all fail data out from said fail location latches of said diagnostic register device are read;

automatically switching, in response to said received de-asserted first signal, said BIST clock control logic to resume data capture at said fail location latches of said diagnostic register device at said high speed multiplied clock; and,

resuming the BIST testing with the high speed multiplied clock from the point at which it was paused, wherein diagnostic bit fail data is extracted from said diagnostic register device without disturbing a state of said BIST or said embedded memory.

Respectfully, no new matter is being entered by this claim and full support is found in the specification and each of the figures. It is understood that Claim 1 incorporates in part, the subject matter as claimed in Claim 5 now canceled.

Claim 1, as now amended herein, clearly tracks functionality as depicted in the method steps as outlined in Fig. 7 of the present specification that highlights a streamlined BIST-Tester interface. This timing diagram of FIG. 7 describes this sequence: embedded memory BIST Test -> Fail Discovered / diagnostic register device captures fail data (CFD=1) -> Test Paused / Tester Alerted (FAIL NET=1) -> Tester Acknowledges Fail / diagnostic register device reconfigured for serial transfer (TII = 1) -> serial unload occurs (SHIFT NET = 1) -> Test resumes (SHIFT NET = 0). This sequence is clearly described in the present specification at paragraphs [0040]-[0044] (referencing the circuit diagrams) and [0051]- [0056] (referencing the timing diagram). Respectfully, amended Claim 1 clearly describes this method.

The recitation of an asserted first signal and de-asserted first signal relate to the "TII" signal asserted by and received from the tester which comprises a handshake mechanism for implementing BIST logic control functionality for asserting SHIFT NET and related shifting out of fail map data as depicted in FIGs. 3-7 of the present application.

Moreover, the recitation that the diagnostic fail data is stored in fail location latches of said diagnostic register device at a time of recognizing said BIST fail test finds original support in the originally filed specification, e.g., in paragraph [0025] which states that "the exact location of the fail is already stored in latches by the time the fail is recognized."

One important claimed feature of the invention is the performance of the BIST testing, performed under control of the high speed multiplied clock which is an asynchronous multiple of a slower external clock (i.e., a multiple of an external ATE (tester) clock speed) that generates a fail map data for capture by a diagnostic register device and while the BIST testing is paused upon recognition of a fail of the embedded memory system. The functionality regarding receiving a fail indication by the BIST engine is fail is now set forth in amended Claim 1 as follows:

> generating a signal for receipt by said tester to identify a BIST bit fail test for said tester, and;
>
> in response to said generated signal, implementing a BIST clock control logic for automatically pausing the BIST bit fail testing upon recognition of a fail of the embedded memory system, said BIST clock control logic gating off said high speed multiplied clock to BIST engine test latches and fail location latches of said diagnostic register;
>
> receiving, from said tester, a first signal asserted in response to receiving said generated signal;
>
> said BIST clock control logic automatically switching, in response to said received asserted first signal, said diagnostic register device to operate from a data capture mode controlled by the high speed multiplied clock to a serial transfer mode controlled by the slower external clock of the tester; and
>
> using the slower external clock of the tester to read bit fail data out from said fail location latches of said diagnostic register device to the tester; and,

The functionality regarding resuming BIST engine testing seamlessly after reading out the fail map data to the external tester (slower) clock speed in the manner as claimed in amended Claim 1 is set forth in Claim 1 as follows:

> receiving, from said tester, a de-asserted first signal when all fail data out from said fail location latches of said diagnostic register device are read;
>
> automatically switching, in response to said received de-asserted first signal, said BIST clock control logic to resume data capture at said fail location latches of said diagnostic register device at said high speed multiplied clock; and,
>
> resuming the BIST testing with the high speed multiplied clock from the point at which it was paused.

What differentiates the present amended Claim 1 from the Nadiau-Dostie prior art is:

1) The fact that the fail map data collected in the claimed diagnostic register device at the multiplied clock speed is read out from the same diagnostic register device at a slower clock speed during the BIST bit fail test pause; and,
2) the diagnostic fail data is stored in fail location latches of said diagnostic register device at a time of recognizing said BIST fail test. This enables heretofore argued functionality that the same diagnostic register device receiving/storing fail map data is used to shift out the data to the external tester;
3) BIST testing is actually paused (BIST clock control logic automatically pauses the BIST bit fail testing upon recognition of a fail of the embedded memory system;
4) The BIST clock control logic gates off the high speed multiplied clock to BIST engine test latches and fail location latches of said diagnostic register during the BIST test pause
5) BIST bit fail data transfer performed in the manner as claimed enables diagnostic bit fail data to be extracted from the diagnostic register device without disturbing a state of said

BIST or said embedded memory. Contrarily, in Nadieau-Dostie, data compression and a copy operation must first be performed before transferring data out.

More particularly, as provided now in more detail, the present invention, as claimed in amended Claim 1, distinguishes over the cited Nadeau-Dostie reference as follows:

1) Nadeau-Dostie must first perform an additional transfer operation: i.e., a copy of the failure summary data from a data selector/encoder to a transfer register. See first sentence in Paragraph [0089] of Nadeau-Dostie. That is, Nadeau-Dostie uses two main registers. Particularly, Figure 8 in Nadeau-Dostie shows a Failure Address Register 176 that captures failing data information. This data is copied to a second Transfer Register 180 for transfer to the tester. Contrarily, in the present invention, the fail map data collected in the claimed fail location latches of the diagnostic register device (at the multiplied clock speed) is read out to the tester from the SAME diagnostic register device at a slower clock speed during the BIST bit fail test pause. This is claimed in Claim 1 as follows:

> said BIST clock control logic automatically switching, in response to said received asserted first signal, said diagnostic register device to operate from a data capture mode controlled by the high speed multiplied clock to a serial transfer mode controlled by the slower external clock of the tester; and
>
> using the slower external clock of the tester to read bit fail data out from said fail location latches of said diagnostic register device to the tester

2) Nadeau-Dostie does not pause BIST bit fail testing as now claimed by its assertion in paragraph [0090] that "the failure summary which is transmitted corresponds to the previous column (or row) tested. The transfer is performed concurrently with the test of a new column or row..." Respectfully, this certainly implies there is no BIST test pause conducted in Nadeau-

Dostie as fail data transfer corresponding to a prior column/row occurs while testing the current column/row.

3) As Nadeau-Dostie does not pause BIST bit fail testing there is no need to implement the BIST clock control logic to gate off said high speed multiplied clock to BIST test latches and fail location latches of said diagnostic register as set forth in the present invention.

4) Nadeau-Dostie does not perform a "handshaking" operation as claimed in the present invention of Claim 1 to inform the external tester that fail location data is available to be serially read-out, to wit:

> generating a signal for receipt by said tester to identify a BIST bit fail test for said tester (as shown by the MUX 15 output 0 → 1 level transition, Figs, 2 and 3)
>
> receiving, from said tester, a first signal asserted in response to receiving said generated signal; (TII signal)
>
> said BIST clock control logic automatically switching, in response to said received asserted first signal, said diagnostic register device to operate from a data capture mode controlled by the high speed multiplied clock to a serial transfer mode controlled by the slower external clock of the tester;

That is, the method of the present invention allows for all diagnostic fails data (every single fail regardless of the number of fails) to be captured and transferred to the tester in a single test pass, i.e., as long as the first signal is asserted by the tester (TII signal, FIG. 7) to control the BIST control logic.

This "handshaking" functionality is not necessary in Nadeau-Dostie as a counter and finite state machine is implemented to control the unloading of the transfer register as the tester

has knowledge of the BIST test patterns. This is not the case in the present invention, i.e., as failure data is captured independent of the BIST test pattern being run or executed.

5) Nadeau-Dostie concentrates on methods for fail compression when reading out column/row bit fail information and the tester must have knowledge of the BIST Test patterns to conduct the failure data read-out. The present invention focuses on BIST-tester interaction during diagnostic data collection as now recited in further detail in amended Claim 1. The difference here is that the purpose of the present invention focuses on automatically stopping/starting BIST test to obtain bit fail map information and as such focuses on circuits/methods that enable this feature with the least overhead in test time/area possible and how this method works with the tester. That is, diagnostic bit fail data is extracted from said diagnostic register device without disturbing a state of said BIST or said embedded memory.Nadeau-Dostie's purpose is to claim advances in fail data compression and NOT for the purpose of improving the interaction between the BIST and tester during fail data collection.

Thus, with respect to the method Claim 1, as amended, this claims significantly differ from Nadeau-Dostie and clearly overcomes any novelty rejection under 35 U.S.C. 102(e). Thus, the Examiner is respectfully requested to withdraw the rejections of amended Claim 1, and withdraw rejections of remaining independent Claims 13 and 21 which have been similarly amended to track recitations added to amended Claim 1.

Claim 6 is being further amended to change its dependency and to track changes made to independent Claim 1 and, Claim 16 is being further amended to change its dependency and to track changes made to independent Claim 13.

In view of the foregoing, the applicants submit that amended Claims 1, 13, and 21 set forth novel subject matter as each element is neither taught nor described by Nadeau-Dostie, whether taken alone or in combination with Hirabayashi

In view of the foregoing, this application is now believed to be in condition for allowance, and a Notice of Allowance is respectfully requested. If the Examiner believes a telephone conference might expedite prosecution of this case, it is respectfully requested that he call applicant's attorney at (516) 742-4343.

Respectfully submitted,

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